US005925133A

United States Patent [19]

Buxton et al.

[11] **Patent Number: 5,925,133**

[45] **Date of Patent: Jul. 20, 1999**

[54] **INTEGRATED PROCESSOR SYSTEM ADAPTED FOR PORTABLE PERSONAL INFORMATION DEVICES**

[75] Inventors: **Clark L. Buxton; Donald G. Craycraft**, both of Austin; **Keith G. Hawkins**, Dripping Springs; **Gary Baum**, Austin, all of Tex.

[73] Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, Calif.

[21] Appl. No.: **08/866,373**

[22] Filed: **May 30, 1997**

Related U.S. Application Data

[63] Continuation of application No. 08/325,661, Oct. 19, 1994, abandoned.

[51] **Int. Cl.**[6] **G06F 1/32**; G06F 1/06

[52] **U.S. Cl.** **713/323**; 713/330; 713/501; 713/600; 713/601

[58] **Field of Search** 395/800.01, 750.01, 395/750.04, 750.06, 555, 556, 750.03, 559, 560

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,083,266	1/1992	Watanabe .	
5,167,024	11/1992	Smith et al.	395/750.04
5,365,183	11/1994	Mitsuhira	327/144
5,369,771	11/1994	Gettel	395/750.04
5,381,543	1/1995	Blomgren et al.	395/550
5,394,515	2/1995	Lentz et al.	395/115
5,418,969	5/1995	Matsuzaki et al.	395/750.04
5,438,681	8/1995	Mensch, Jr.	395/800
5,481,697	1/1996	Mathews et al.	395/550
5,493,684	2/1996	Gephardt et al.	395/750
5,495,422	2/1996	Olson	364/491
5,511,209	4/1996	Mensch, Jr.	395/800
5,513,374	4/1996	Baji	395/846
5,537,581	7/1996	Conary et al.	395/550

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

0 208 287	1/1987	European Pat. Off. .
0 364 222	4/1990	European Pat. Off. .
0 391 543	10/1990	European Pat. Off. .

OTHER PUBLICATIONS

Electronic News, "National Melds LAN, I/O Devices", Jul. 25, 1994.

Nass, "PC Chip Integrater LAN Functionality", *Electronic Design*, Jul. 1994, pp. 141–142.

Nass, R., "Subnotebook Systems Minimize Trade-Offs Portable-System Designers Try to Reduce Size, Weight, Power Consumption, and Cost While Increasing Performance," Electronic Design, vol. 41, No. 16, Aug. 5, 1993, pp. 57, 58, 62, 64, 66–68.

(List continued on next page.)

Primary Examiner—Meng-Ai T. An
Assistant Examiner—Walter D. Davis, Jr.
Attorney, Agent, or Firm—Conley, Rose & Tayon; Robert C. Kowert; Kevin L. Daffer

[57] **ABSTRACT**

An integrated processor is fabricated on a single monolithic circuit and employs circuitry to accommodate data-intensive, view-intensive and voice-intensive requirements of modern-day PIDs. The integrated processor includes a CPU core, a memory controller, and a variety of peripheral devices to achieve versatility and high performance functionality. The integrated processor consumes less power by provision of a clock control unit including a plurality of phase-locked loops for generating clock signals of differing frequencies to appropriately clock the various subsystems of the integrated processor. The clock signals provided to the various subsystems by the clock control unit are derived from a single crystal oscillator input signal. A power management unit is incorporated within the integrated processor to control the frequency and/or application of certain clock signals to the various subsystems, as well as to control other power management related functions. The pin-count of the integrated processor is finally minimized by allowing the selective multiplexing of certain external pins depending upon the desired functionality of the integrated processor.

17 Claims, 5 Drawing Sheets